Collaboration Projects

Spatial-Temporal Multiplexing Packet Radio Signal Transmission Technologies

For the purpose of establishing new system technologies focusing on adaptive signal processing, we conducted research on radio signal processing algorithms for packet-based communication. This research was conducted jointly with the Suzuki & Fukawa laboratory (Professor Hiroshi Suzuki and Associate Professor Kazuhiko Fukawa), Graduate School of Science and Engineering, Tokyo Institute of Technology.

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1. Introduction

Driven by the recent remarkable diffusion of mobile communication represented by mobile phones and strong demand for shift to multimedia contents, the technical requirements placed on data, image and other large-volume forms of digital signal transmission are increasing. Moreover, in order to realize seamless Internet access that can match the quality of fixed networks, it is necessary to establish random access technologies in packet-based wireless communication, which are integrated with high-speed transmission technologies. In this research, we examined various algorithms, in particular adaptive signal processing algorithms, for the purpose of establishing new system technologies that will enable us to construct random access mobile communication systems with high spectral efficiency.

Specifically, we focused on Multiple Input Multiple Output (MIMO) communication, which allows high-speed transmission without requiring a wider signal bandwidth by conducting spatial division multiplexing using multiple reception/transmission antennas, and examined a method that increases the channel capacity further by utilizing the channel state information on the transmission side. We mainly examined the following technologies.

1) A proposal of applying phase hopping diversity to MIMO-Orthogonal Frequency Division Multiplexing (MIMO-OFDM) transmission, thus allowing spatially multiplexing transmission and improving the decoding performance of error correcting codes
2) A proposal of a timing recovery method with a high-precision path detector for OFDM, taking application to high-speed MIMO-OFDM communication into consideration
3) A proposal of a multi-user detector for OFDM transmission adopting metric-combining Automatic Repeat reQuest (ARQ) that allows high-reliability packet transmission
4) A proposal of a MIMO-OFDM turbo equalizer that allows highly reliable signal transmission even in multipath propagation environments with large delays
5) Investigation of the Time Division Duplex (TDD) transmission technology, which has the characteristic that the channel state information can easily be utilized on the transmission side

Among the technologies above, this article provides an overview of the phase hopping diversity method and the timing recovery method with a high-precision path detector [1] [2].

2. Phase Hopping Diversity Method

2.1 Algorithm Overview

In OFDM transmission, which is highly robust against multipath interference, the channel gain fluctuations vary for each subcarrier in a frequency-selective fading environment; it is thus possible to obtain a frequency diversity effect by utilizing error correcting code and similar. In adjacent subcarriers, however, the channel gain fluctuations are likely to be similar and it is not possible to obtain a sufficient frequency diversity effect.

To alleviate this problem, the phase hopping diversity method, which improves the error rate performance due to the transmit diversity effects brought about by assigning a different phase shift to each transmission antenna, can be applied to each subcarrier in an OFDM signaling. In this Subcarrier Phase

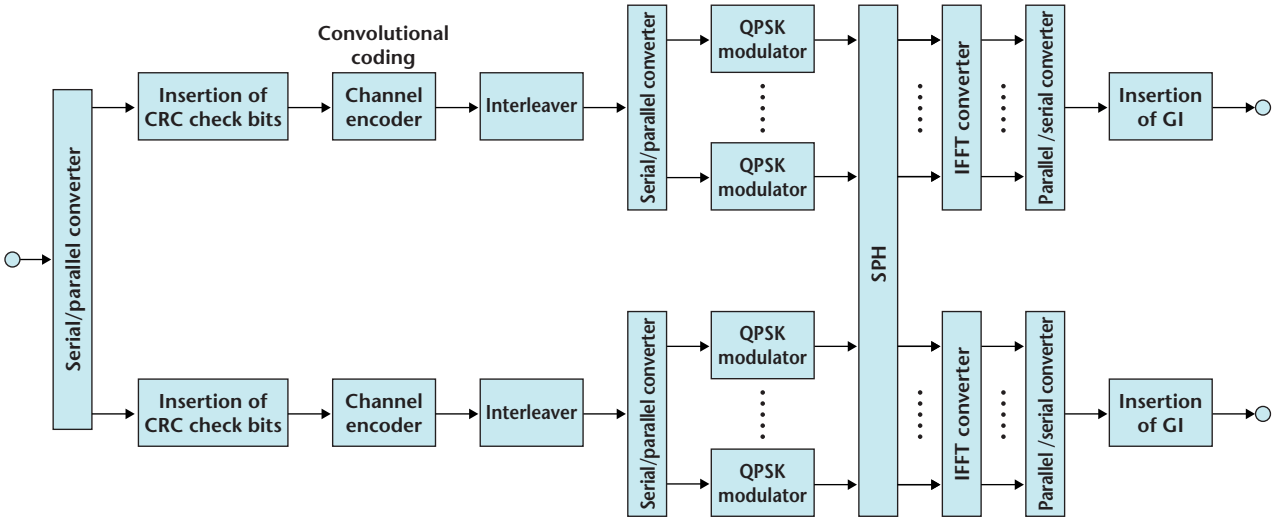

Figure 1 Configuration of MIMO-OFDM transmitter using SPH

Hopping (SPH) method, the received signal gain of each subcarrier can be changed independently by assigning a phase rotation to each subcarrier independently at transmission. It is thus possible to decrease the probability that the reception power of adjacent subcarriers drops significantly at the same time. Consequently, it is possible to improve the reception performance by avoiding situations where encoded bits continually become erroneous and it is difficult to correct errors when error correction codes are used.

Figure 1 shows a configuration of a MIMO-OFDM transmitter using SPH when two transmission antennas are used. On the transmitter side, Cyclic Redundancy Check (CRC) bits are added to the data and then coding, interleaving and mapping are performed. In normal OFDM transmitters, the Inverse Fast Fourier Transform (IFFT) is then applied. In this method, however, the signals of each subcarrier are multiplied by a random phase matrix. After this random phase multiplication, the IFFT is applied and Guard Intervals (GI) are inserted into the signals, which are then transmitted.

At this point, it is possible to prevent the performance degradation when detecting the transmission signals to which the SPH method is applied on the receiver side by utilizing random phase matrices that are orthogonal to each other. Moreover, the receiver does not require any information about the phase shift applied on the transmission side.

2.2 Performance Evaluation

In order to verify the effectiveness of the algorithm, we implemented the algorithm on a evaluation board equipped with multiple Field Programmable Gate Arrays (FPGA)* using Hardware Description Language (HDL). This section provides an overview of the FPGA board and shows the result of validating the proposed algorithm using the FPGA board.

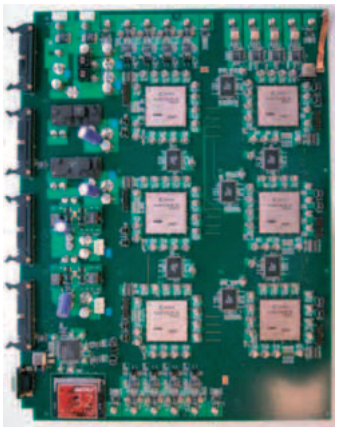

Photo 1 External view of FPGA evaluation board

1) Overview of FPGA Boards

Photo 1 shows the external view of the FPGA evaluation board used in this research. This board has six FPGAs with approximately seven million system gates each and it is thus able to implement logic using a total of 42 million system gates on the board as a whole. Each FPGA is equipped with 328 multipliers and excellent Multiply and ACcumulate (MAC) performance can be achieved. Each FPGA is equipped with 2 MB high-speed access Zero Bus Turnaround-Synchronous Static Random Access Memory (ZBT-SSRAM), which is used for

* FPGA: A programmable large-scale integrated circuit composed of cells arranged in an array pattern, interlinked with wiring devices. Since it is basically a hardware device, it has characteristics of high speed and low power consumption, yet the functionality can easily be changed by modifying the circuit.

data exchange between the FPGAs and implementing the required function tables. The Analog to Digital (A/D) and Digital to Analog (D/A) converter on the board have a resolution of 14 bits and operate at 105 Msps (samples per second) and 160 Msps, respectively. Each A/D converter has two channels for In-phase (I) and Quadrature-phase (Q) signals (four channels in total) and each D/A converter has four channels for I and Q signals (eight channels in total), which are used for monitoring.

2) Experimental Results

We conducted a laboratory experiment in the digital baseband domain using the aforementioned FPGA board. The basic specifications of this experiment are shown in **Table 1**. We evaluated the effects of applying SPH in both 2×2 (2 transmission antennas and 2 reception antennas) MIMO and 2×1 Multiple Input Single Output (MISO) transmission. We also evaluated the SPH-Transmit Diversity (TD) method, which uses transmit diversity for the SPH method, for the sake of comparison. The circuit scale required for implementing the SPH method in the 2×2 MIMO system was approximately 1/20 of the transmission/reception processing circuit as a whole and 1% of the FPGA board as a whole (420,000 gates).

Figure 2 shows the spectrum of the received signals measured with a spectrum analyzer. As the figure shows, it is possible to avoid the significant reception level attenuation in a wide range from the center frequency (0 Hz on the horizontal axis) toward the lower frequencies of 20 MHz observed in the 2-path Rayleigh fading environment by applying the SPH method.

Figure 3 shows the Packet Error Rate (PER) performance in a 16-path Rayleigh fading environment obtained by the FPGA board, compared with similar results obtained in computer simulation. The PER performance obtained by the FPGA board agreed well with the performance obtained in computer simulation. Compared with conventional methods where SPH is not applied, in the 2×2 MIMO system, it is possible to reduce

Table 1 Basic specifications

Encoding/modulation method	OFDM/QPSK (coding rate: 1/2)
Number of FFT points	64
Number of subcarriers	52 (data: 48, pilot: 4)
Bandwidth	80 MHz
Number of antennas	Transmitter: 2, receiver: 1 or 2
Transmission rate	TD: 48 Mbit/s, SDM: 96 Mbit/s
Propagation model	16-path exponentially decayed Rayleigh fading model

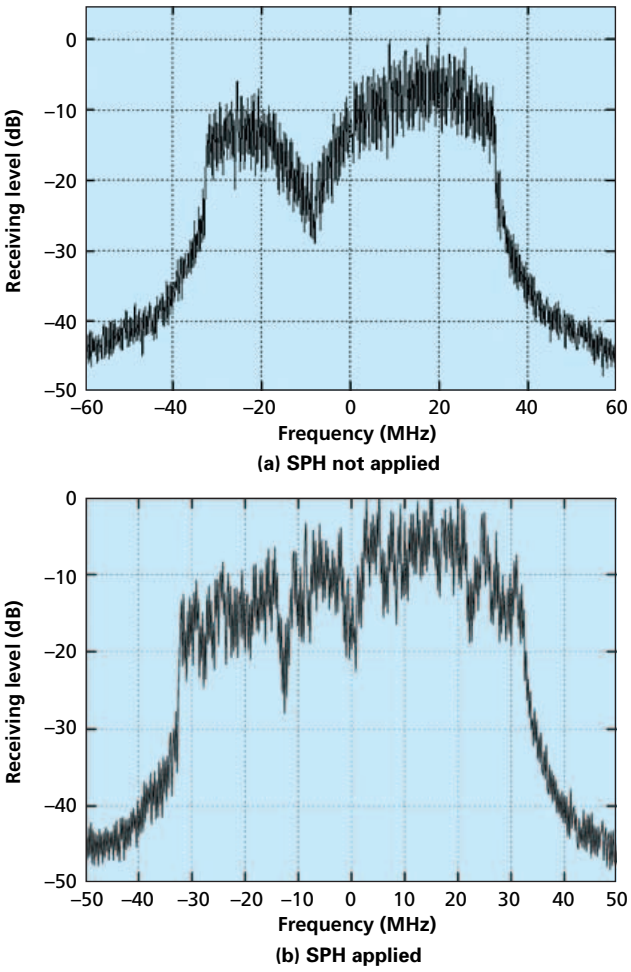

Figure 2 Spectrum with/without SPH

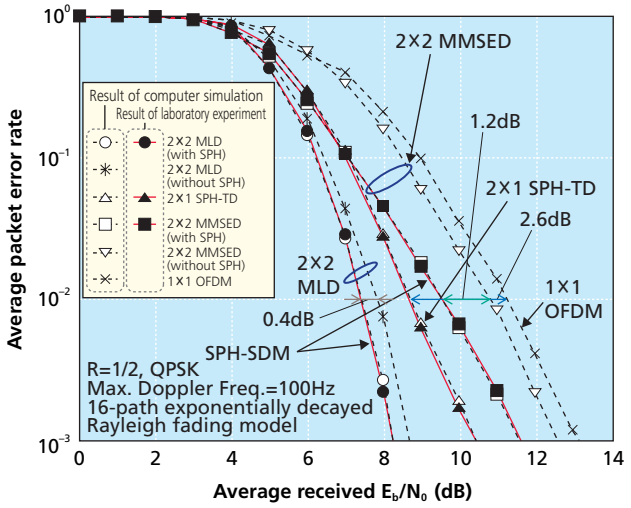

Figure 3 Average packet error rate performance

the required E_b/N_0 at which a PER of 10^{-2} can be achieved by 0.4 dB if a Maximum Likelihood Detection (MLD) algorithm is used for the detection algorithm, and by 1.2 dB if a Minimum Mean Squared Error Detection (MMSED) approach is used, by applying SPH-Spatial Division Multiplexing (SDM). Moreover,

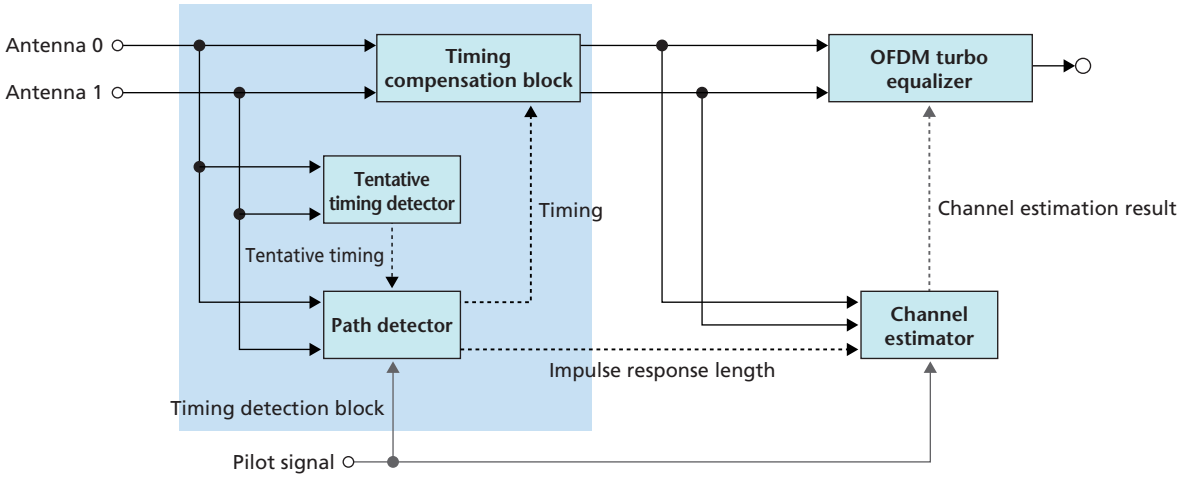

Figure 4 Timing recovery method using high-precision path detector

it was confirmed that the required E_b/N_0 where a PER of 10^{-2} is achieved can be reduced by 2.6 dB by applying the SPH-TD method compared to a 1 X 1 OFDM system.

3. Timing Recovery Method Using High-Precision Path Detector

When OFDM transmission is used, it is necessary to determine the timing for the Fast Fourier Transform (FFT) window before carrying out the FFT processing in a receiver. In conventional methods, the timing is determined by calculating the auto-correlation of the received signals using the guard interval's periodicity. In the proposed method, however, the detection of the reception timing is improved by performing the following processing as well (**Figure 4**).

First, the path detector estimates the channel impulse response based on the timing obtained in conventional auto-correlation processing with a tentative timing detector. Then, based on the channel impulse response, it compensates for the timing error such that the position of the first path is within the FFT window. Furthermore, it notifies the length of the channel impulse response to the subsequent channel estimator to improve the channel estimation accuracy.

Since the estimated impulse response includes noise components, it is necessary to distinguish the impulse response from the noise to estimate the number of paths accurately. In order to address this issue, the noise power in the received signals is estimated and signal components with greater power than the noise power are regarded as effective paths to estimate the number of paths. Following this, the timing is adjusted such that all the multipath components are included. Since the power of delayed paths is likely to be lower than that of the first path, a different threshold value from the value used for timing compensation is used.

As a result of PER performance evaluation by computer simulation, it is confirmed that it is possible to reduce the required E_b/N_0 where a PER of 10^{-1} can be achieved by 3 dB by using this method.

4. Conclusion

This article provided an overview of two new packet-based radio signal transmission technologies, focusing on adaptive signal processing. We are continuously examining new technologies that will allow for highly reliable high-speed transmission and will pursue investigating how these technologies can be applied for future mobile communication systems as well.

REFERENCES

[1] S. Suyama, K. Tochihara, H. Suzuki and K. Fukawa: "A MIMO-OFDM transmission scheme employing subcarrier phase hopping," 5th Int'l Workshop on Multi-Carrier Spread Spectrum (MC-SS), Oberpfaffenhofen, Germany, Sep. 2005.

[2] T. Shizuno, S. Suyama, H. Suzuki and K. Fukawa: "An Accurate OFDM timing recovery with timing offset compensation by channel estimation results for mobile packet transmission," The First IEEE Asia Pacific Wireless Communi. Sympo. (APWCS), Seoul, Korea, pp. 16–20, Jan. 2004.

ABBREVIATIONS

A/D: Analog to Digital
ARQ: Automatic Repeat reQuest
CRC: Cyclic Redundancy Check
D/A: Digital to Analog
FFT: Fast Fourier Transform
FPGA: Field Programmable Gate Array
GI: Guard Interval
HDL: Hardware Description Language
IFFT: Inverse FFT
MAC: Multiply and ACcumulate
MIMO: Multiple Input Multiple Output
MISO: Multiple Input Single Output
MLD: Maximum Likelihood Detection
MMSED: Minimum Mean Squared Error Detection
OFDM: Orthogonal Frequency Division Multiplexing
PER: Packet Error Rate
SDM: Spatial Division Multiplexing
SPH: Subcarrier Phase Hopping
TD: Transmit Diversity
TDD: Time Division Duplex
ZBT-SSRAM: Zero Bus Turnaround-Synchronous Static Random Access Memory